WHAT IS CLAIMED IS:

1. A circuit, comprising:

a comparing means for comparing an internal voltage to a reference voltage for outputting a first driving signal;

an internal voltage driving means for outputting the internal voltage in response to the first driving signal;

an internal voltage detecting means for detecting the internal voltage and for generating a second driving signal in response to an active signal; and

an overdriving control means for controlling the first driving signal in response to the second driving signal.

2. The circuit of claim 1, wherein the internal voltage driving means includes a PMOS transistor.

3. The circuit of claim 1, wherein the overdriving control means includes an NMOS transistor having a drain connected to an output terminal of the comparing means, a gate for receiving the second driving signal, and a source connected to a ground voltage.

4. The circuit of claim 1, wherein the active signal is a pulse signal having a predetermined pulse width.

5. The circuit of claim 1, wherein the internal voltage detecting means inactivates the second driving signal when the active signal is inactivated, activates the second driving signal when the active signal is activated and the internal voltage is less than or equal to a target voltage, and inactivates the second driving signal when the active signal is activated and the internal voltage is greater than the target voltage.

6. The circuit of claim 1, wherein the internal voltage detecting means outputs the second driving signal at a low level when the active signal is at the low level, outputs the second driving signal at a high level when the active signal is at the high level and the internal voltage is less than or equal to a target voltage, and outputs the second driving signal at the low level when the active signal is at the high level and the internal voltage is greater than the target voltage.

7. The circuit of claim 1, wherein the internal voltage detecting means includes:

a first inverter for inverting the active signal to generate an inverted active signal, wherein the first inverter is connected between the internal voltage and a ground voltage;

a second inverter for inverting the inverted active signal, wherein the second inverter is connected between the internal voltage and the ground voltage;

a first voltage generating circuit for receiving an output signal of the second inverter and for outputting a first voltage derived from the output signal;

a first transistor connected to the internal voltage, wherein the first transistor is turned on to activate the second driving signal in response to the inverted active signal;

a second transistor connected to a ground voltage, wherein the second transistor is turned on to inactivate the second driving signal when the first voltage is greater than a predetermined voltage; and

a switching transistor, wherein the switching transistor is turned onto inactivate the second driving signal in response to the inverted active signal.

8. The circuit of claim 7, wherein the first transistor includes a source for receiving the internal voltage, a gate for receiving the inverted active signal, and a drain for outputting the second driving signal.

9. The circuit of claim 7, wherein the second transistor includes a source for receiving the ground voltage, a gate for receiving the first voltage, and a drain for outputting the second driving signal.

10. The circuit of claim 7, wherein the switching transistor includes a gate for receiving the inverted active signal, a source connected to the ground voltage, and a drain for outputting the second driving signal.

11. A circuit, comprising:

a first comparing means for comparing an internal voltage to a reference voltage for outputting a first driving signal;

an internal voltage driving means for outputting the internal voltage in response to the first driving signal;

a voltage dividing means for dividing the internal voltage to generate a divided voltage in response to an active signal;

a second comparing means for comparing the divided voltage to the reference voltage for generating a second driving signal; and

an overdriving control means for controlling the first driving signal in response to the second driving signal.

12. The circuit of claim 11, wherein the internal voltage driving means includes a PMOS transistor.

13. The circuit of claim 11, wherein the overdriving control means includes an NMOS transistor having a drain connected to an output terminal of the first comparing means, a gate for receiving the second driving signal, and a source connected to a ground voltage.

14 The circuit of claim 11, wherein the active signal is a pulse signal having a predetermined pulse width.

15. The circuit of claim 11, wherein the voltage dividing means outputs the internal voltage when the active signal is inactivated, and divides the internal voltage to generate the divided voltage when the active signal is activated.

16. The circuit of claim 15, wherein:

the divided voltage is less than the reference voltage when the internal voltage is less than or equal to a target voltage; and

the divided voltage is greater than the reference votlage when the internal voltage is greater than the target voltage.

17. The circuit of claim 11, wherein the voltage dividing means outputs the internal voltage when the active signal is at a low level, and divides the internal voltage to generate the divided voltage when the active signal is at a high level.

18. The circuit of claim 11, wherein the voltage dividing means includes:

a first load connected to the internal voltage and a first node;

a second load connected between the first node and a second node; and

a switching transistor having a drain connected to the second node, a gate for receiving the active signal, and a source connected to a ground voltage,

wherein the divided voltage is generated through the first node.

19. The circuit of claim 18, wherein the switching transistor includes an NMOS transistor.

20. The circuit of claim 11, wherein the second comparing means inactivates the second driving signal when the active signal is inactivated, and compares the divided voltage to the reference voltage when the active signal is activated for activating the second driving signal when the divided voltage is less than the reference voltage

and for inactivating the second driving signal when the divided voltage is greater than the reference voltage.

21. The circuit of claim 11, wherein the second comparing means outputs the second driving signal at a low level when the active signal is at the low level, and compares the divided voltage to the reference voltage when the active signal is at a high level for outputting the second driving signal at the high level when the divided voltage is less than the reference voltage and for outputting the second driving signal at the low level when the divided voltage is greater than the reference voltage.

22. The circuit of claim 11, wherein the second comparing means includes:

a first inverter for inverting the active signal to generate an inverted active signal;

a switching transistor for inactivating the second driving signal in response to the inverted active signal; and

a comparator for comparing the divided voltage to the reference voltage for activating the second driving signal when the divided voltage is less than the reference voltage and for inactivating the second driving signal when the divided voltage is greater than the reference voltage.

23. The circuit of claim 22, wherein the switching transistor includes a gate for receiving the inverted active signal, a source connected to a ground voltage, and a drain for outputting the second driving signal.

24. A circuit, comprising:

a comparing means for comparing a comparison voltage to a reference voltage to generate a first driving signal;

an internal voltage driving means for outputting an internal voltage in response to the first driving signal; and

a voltage dividing means for receiving the internal voltage, for generating, in response to an active signal, the comparison voltage having a value equal to the internal voltage during a normal driving operation, and for dividing, in response to the active signal, the internal voltage to generate the comparison voltage having a value equal to the divided internal voltage during an overdriving operation.

25. The circuit of claim 24, wherein the internal voltage driving means includes a PMOS transistor.

26 The circuit of claim 24, wherein the active signal is a pulse signal having a predetermined pulse width.

27. The circuit of claim 24, wherein the voltage dividing means outputs the comparison voltage equal to the internal voltage when the active signal is inactivated, and divides the internal voltage to generate the comparison voltage equal to the divided internal voltage when the active signal is activated.

28. The circuit of claim 27, wherein

the divided internal voltage is less than the reference voltage when the internal voltage is less than or equal to a target voltage; and

the divided internal voltage is greater than the reference voltage when the internal voltage is greater than the target voltage.

29. The circuit of claim 24, wherein the voltage dividing means outputs the comparison voltage equal to the internal voltage when the active signal is at a low level, and divides the internal voltage to generate the comparison voltage equal to the divided internal voltage when the active signal is at a high level.

30. The circuit of claim 24, wherein the voltage dividing means includes:

a first load connected to the internal voltage and a first node;

a second load connected between the first node and a second node; and

a switching transistor having a drain connected to the second node, a gate for receiving the active signal, and a source connected to a ground voltage,

wherein the divided internal voltage is generated through the first node.

31. The circuit of claim 30, wherein the switching transistor includes an NMOS transistor.

32. A voltage generating method, comprising:

comparing an internal voltage to a reference voltage to generate a first driving signal;

outputting the internal voltage in response to the first driving signal;

detecting the internal voltage and outputting a second driving signal in response to an active signal; and

controlling the first driving signal in response to the second driving signal.

33. The method of claim 32, further comprising:

inactiviating the second driving signal when the active signal is inactivated;

activating the second driving signal when the active signal is activated and the internal voltage is less than or equal to a target voltage; and

inactivating the second driving signal when the active signal is activated and the internal voltage is greater than the target voltage.

34. The method of claim 32, further comprising:

outputting the second driving signal at a low level when the active signal is at the low level;

outputting the second driving signal at a high level when the active signal is at the high level and the internal voltage is less than or equal to a target voltage; and

outputting the second driving signal at a low level when the active signal is at the high level and the internal voltage is greater than the target voltage.